Serial No. 10/074,533
Docket No. CS10721

REMARKS

In the office action, the Examiner rejected claims 5, 7, 8, 11-12 and 17 under 35 U.S.C. Section 112, second paragraph, "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." It is respectfully submitted that the claim clearly define applicant's invention. Reconsideration of the claims as presented herein is respectfully requested.

Claims 1-6, 9-11, and 14-15 are rejected under 35 U.S.C. section 102(e) as being anticipated by Ma et al. ('880). Claims 13 and 16 were objected to as being dependent upon a rejected base claim. Claims 13 and 16 are rewritten in independent form, and are now in condition for allowance. In view of the following comments, the rejection of claims 1-6, 9-11 and 14-15 is respectfully traversed, and reconsideration of the claims as presented herein is respectfully requested.

Ma discloses an integrated circuit having a limited number of pins wherein I/O ports are shared by a master core and at least one slave core. A configurable interconnect 100 is responsive to control bits from the master core to control direction. The interconnect control is also connected to the port to select pull-up or pull-down control of the port. The configurable interconnect 100 also generates interrupts which are communicated back to the cores. However, Ma fails to show or suggest a logical configuration block, a method of combing control bits to produce resulting control bits, generating a shared subset of control bits, or providing a resultant set of bits as control bits to a slave peripheral unit.

According to one aspect of the present invention, a logic configuration block controls the generation of a resultant shared subset of control bits for the slave peripheral unit according to a logical combination set by configuration bits from the first master control unit. According to another aspect, a logic configuration block coupled to first and second input registers and a configuration register to control generation of a shared subset of control bits for the slave peripheral unit, the logic block configurable by a set of configuration bits from the configuration register. According to yet another aspect of the invention, a logical operation is performed on first and second set of control bits from first and second control units to provide a resultant set of control bits, the resultant control bits for application to a slave

peripheral unit. According to still another aspect of the invention, configuring a logic operation responsive to said at least one logic configuration bit, performing the logical operation on the first and second set of bits to selectively combine the bits according to the configured logic and generate a resultant set of bits, and applying the resultant set of bits as control bits to the slave peripheral unit. According to one other aspect of the invention, a combinational logic block is responsive to logic configuration bits received from the first master control unit for configuring a dynamic logic combination of the first and second sets of bits, and the combinational logic block outputting resultant control bits for the slave device derived from a combination of the first and second sets of bits. Ma is devoid of the claimed structure and neither anticipates nor suggests the claimed invention.

It is respectfully submitted that the claims clearly define the invention, and are in condition for allowance. A Notice of Allowance is respectfully solicited.

Respectfully Submitted

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